CLAIMS

What is claimed is:

1. A method of scheduling upstream data packets utilizing a register interface in a data communication system, wherein the data communication system comprises a current system timer, at least one plurality of upstream hardware registers, and a plurality of upstream data packets, and wherein the upstream data packets have an associated priority value (PV), the method comprising the steps of:
   (a) queuing at least one upstream data packet for transmission over the data communication system;
   (b) identifying a priority value (PV) associated with the queued upstream data packet that has not been previously stored in an upstream hardware register;
   (c) storing the PV identified in step (b) in an available upstream hardware register;
   (d) determining whether any upstream hardware register contains a PV corresponding to a current system timer value; and
   (e) transmitting an upstream data packet that is associated with the PV determined in step (d) to be corresponding to the current system timer value.

2. The method of scheduling upstream data packets as defined in Claim 1, wherein the priority value (PV) comprises a time-to-send (TTS) value.

3. The method of scheduling upstream data packets as defined in Claim 1, wherein the PV comprises a sum of time-to-send (TTS) values and an offset value.

4. The method of scheduling upstream data packets as defined in Claim 1, wherein the PV value includes a control message.

5. The method of scheduling upstream data packets as defined in Claim 1, wherein the transmitting step (e) further includes the step of converting an upstream hardware register associated with the PV determined in step (d) to correspond to the current system timer value to a free upstream hardware register.

6. The method of scheduling upstream data packets as defined in Claim 1, wherein the at least one plurality of upstream hardware registers comprises a parallel hardware register configuration.

7. The method of scheduling upstream data packets as defined in Claim 1, wherein the at least one plurality of upstream hardware registers comprises a serial hardware register configuration.

8. The method of scheduling upstream data packets as defined in Claim 1, wherein the at least one plurality of upstream hardware registers comprises a parallel-serial hardware register configuration.

9. The method of scheduling upstream data packets as defined in Claim 1, wherein the at least one plurality of upstream hardware registers comprises 32 hardware registers.

10. The method of scheduling upstream data packets as defined in Claim 1, wherein an upstream hardware register includes a pointer register and a PV register.

11. The method of scheduling upstream data packets as defined in Claim 1, wherein the data communication system comprises a cable modem communication system.

12. A method of scheduling upstream data packets utilizing a parallel hardware register interface in a data communication system, wherein the data communication system includes a current system timer, a plurality of customer premise equipment (CPE) in communication with at least one associated and corresponding cable modem, and wherein the at least one cable modem has an associated and corresponding cable modem termination system (CMTS), the method comprising the steps of:

(a) receiving new upstream data packets into at least one cable modem;

(b) determining whether the at least one cable modem received a new upstream data packet;

(c) creating a new burst information structure (BIS) and storing a time-to-send (TTS) and pointer value in an upstream hardware register, wherein the TTS and pointer values are associated with corresponding upstream data packets;

(d) determining whether any of the TTS values stored in an associated upstream hardware register corresponds with a current system timer value; and

(e) if any TTS value corresponds with the current system timer value, transmitting an upstream data packet that is associated with the TTS, else returning to step (a).

13. A method of scheduling upstream data packets utilizing a parallel hardware register interface in a data communication system, wherein the data communication system includes a system timer, a plurality of customer premise equipment (CPE) in communication with at least one associated and corresponding cable modem, and wherein the at least one cable modem has an associated and corresponding cable modem termination system (CMTS), the method comprising the steps of:

(a) determining whether a new burst information structure (BIS) has been created;

(b) obtaining an available upstream hardware register from a plurality of upstream hardware registers;

(c) storing information pertaining to an upstream data packet associated with the new BIS in the available upstream hardware register if a new BIS was determined to be created in step (a);

(d) determining whether a time-to-send (TTS) value associated with the plurality of upstream hardware registers corresponds to a current system timer value; and

(e) if any TTS value is associated with the current system timer value, transmitting an upstream data packet that is associated with the TTS, else returning to step (a).

14. The method of scheduling upstream data packets as set forth in Claim 13, wherein the step (b) of obtaining an available upstream hardware register uses a CU_IN_Free_Index register to find finding a free upstream hardware register.

15. The method of scheduling upstream data packets as set forth in Claim 13, wherein the step (b) of obtaining an available upstream hardware register uses a CU_In_DMA_PTR register, a CU_In_DMA_Cnt register and a CU_In_TTS register for storing information pertaining to the available upstream hardware register.

16. An upstream data packet scheduler comprising a hardware register interface in a data communication system, wherein data is communicated using a plurality of upstream data packets, and wherein an upstream data packet has an associated and corresponding priority value (PV), comprising:

(a) an upstream hardware register means, wherein the upstream hardware register means includes available and unavailable hardware registers;

(b) means, coupled to the upstream hardware register means, for queuing upstream data packets for transmission over the data communication system;

(c) means, responsive to the queuing means, for identifying a priority value (PV) associated with a queued upstream data packet that has not been stored in the upstream hardware register means;

(d) means, responsive to the identifying means, for storing the PV identified by the identifying means in an available upstream hardware register;

(e) means for maintaining a current system timer value;

(f) means, operatively coupled to the system timer value means and the upstream hardware register means, for determining whether the hardware register means contains a PV that corresponds to the current system timer value; and

(g) means, responsive to the determining means, for transmitting an upstream data packet that is associated with the PV determined by the determining means to correspond to the current system timer value.

17. An upstream data packet scheduler comprising a hardware register interface for use in a data communication system, wherein the data communication system comprises a system timer, a plurality of upstream hardware registers, and a plurality of upstream data packets, and wherein at least one upstream data packet has an associated and corresponding priority value (PV), comprising:

(a) a PV register reader, wherein the reader determines whether a PV of queued upstream data packets received by a hardware register interface has been stored into an upstream hardware register;

(b) an upstream hardware register writer, operatively coupled to the PV register reader and the plurality of upstream hardware registers, wherein the writer stores a PV associated and corresponding to an upstream data packet into an available upstream hardware register;

(c) a register comparator, operatively coupled to the plurality of upstream hardware registers and the system timer, wherein the comparator determines whether any PV stored in the plurality of upstream hardware registers is associated with a current system timer value; and

(d) said scheduler configured to operate with a transmitter; that is operatively coupled to the register comparator and transmits upstream data packets associated with and corresponding to a PV that is associated with the current system timer value.

18. A method of scheduling upstream data packets utilizing a hardware register interface in a data communication system, wherein the data communication system includes a current system timer, a plurality of upstream hardware registers, and a plurality of upstream data packets, and wherein each upstream data packet has an associated and corresponding priority value (PV), the method comprising the following steps:

(a) a step for queuing upstream data packets for transmission over the data communication system;

(b) a step for identifying a priority value (PV) associated with a queued upstream data packet that has not been previously stored in an upstream hardware register;

(c) a step for storing the PV identified in step (b) in an available upstream hardware register;

(d) a step for determining whether any upstream hardware register contains a PV that corresponds to a current system timer value; and

(e) a step for transmitting an upstream data packet that is associated with the PV determined in step (d) to correspond to the current system timer value.

19. A method of scheduling upstream data packets utilizing a parallel hardware register interface in a data communication system, wherein the data communication system includes a system timer, a plurality of customer premise equipment (CPE) in communication with at least one associated and corresponding cable modem, and wherein the at least one cable modem has an associated and corresponding cable modem termination system (CMTS), the method comprising the following steps:

(a) a step for determining whether a new burst information structure (BIS) has been created;

(b) a step for obtaining an available upstream hardware register from a plurality of upstream hardware registers;

(c) a step for storing information pertaining to an upstream data packet associated with the new BIS in the available upstream hardware register if a new BIS was determined to be created in step (a);

(d) a step for determining whether a time-to-send (TTS) value associated with the plurality of upstream hardware registers corresponds to a current system timer value; and

(e) if any TTS value corresponds to the current system timer value, a step for transmitting an upstream data packet that is associated with the TTS, else returning to step (a).